103Gb/s QSFP28 SR4 Transceiver

APQP2SRA3CDM01

Product Features

- ✓ 4 channels full-duplex transceiver modules
- ✓ 4*25Gb/s 850nm VCSEL-based transmitter
- ✓ 4*25Gb/s electrical interface
- ✓ Power dissipation <2W
- ✓ Hot-pluggable QSFP28 form factor
- ✓ Single MPO connector receptacle
- ✓ Maximum link length of 70m on OM3 or 100m on OM4 multimode fiber (MMF)
- ✓ Operating case temperature 0°C to +70°C
- ✓ 3.3V power supply voltage

Applications

- ✓ 100GBASE-SR4 100G Ethernet
- ✓ Switch, router and HBAs
- ✓ Infiniband transmission at 4 channels SDR, DDR and QDR
- ✓ High-performance Backplane Applications
- ✓ Proprietary Protocol Applications

Product Selection

Part Number	Operating Case temperature	DDMI
APQP2SRA3CDM01	Commercial(0~70℃)	Yes

General Description

This product is an integrated transceiver module containing a micro-optic component and semiconductor material, and can implement optical-electrical conversion and electrical-optical conversion. The module is designed as a four-channel, pluggable, parallel, QSFP28 transceiver for 100Gbps fiber-communication. Each channel can operate at 25Gbps up to 70m on OM3 fiber. And the operating wavelength is 850nm. The optical interface uses an 12 fiber MTP(MPO) connector, and the electrical interface uses a 38 contact edge type connector.

This product is compliant to 100GBASE-SR4 of IEEE802.3bm standard and SFF-8436 specification, and provides reliable long life, high performance, and consistent service

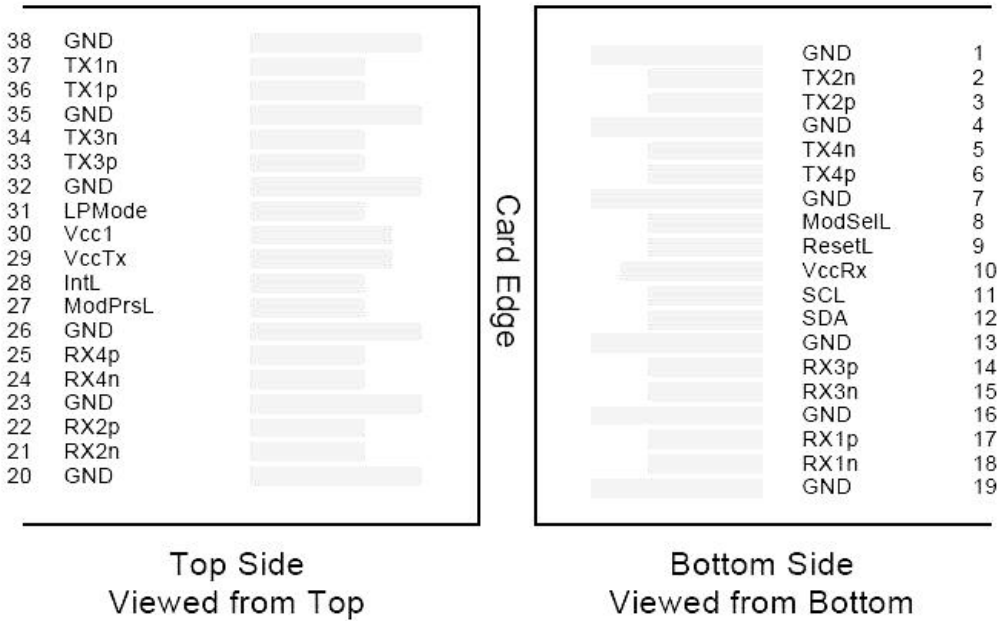
Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- ESD to the MPO connector: compatible with IEC 61000-4-2
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2
- RoHS compliant with RoHS 2 (2011/65/EU)

Pin Descriptions

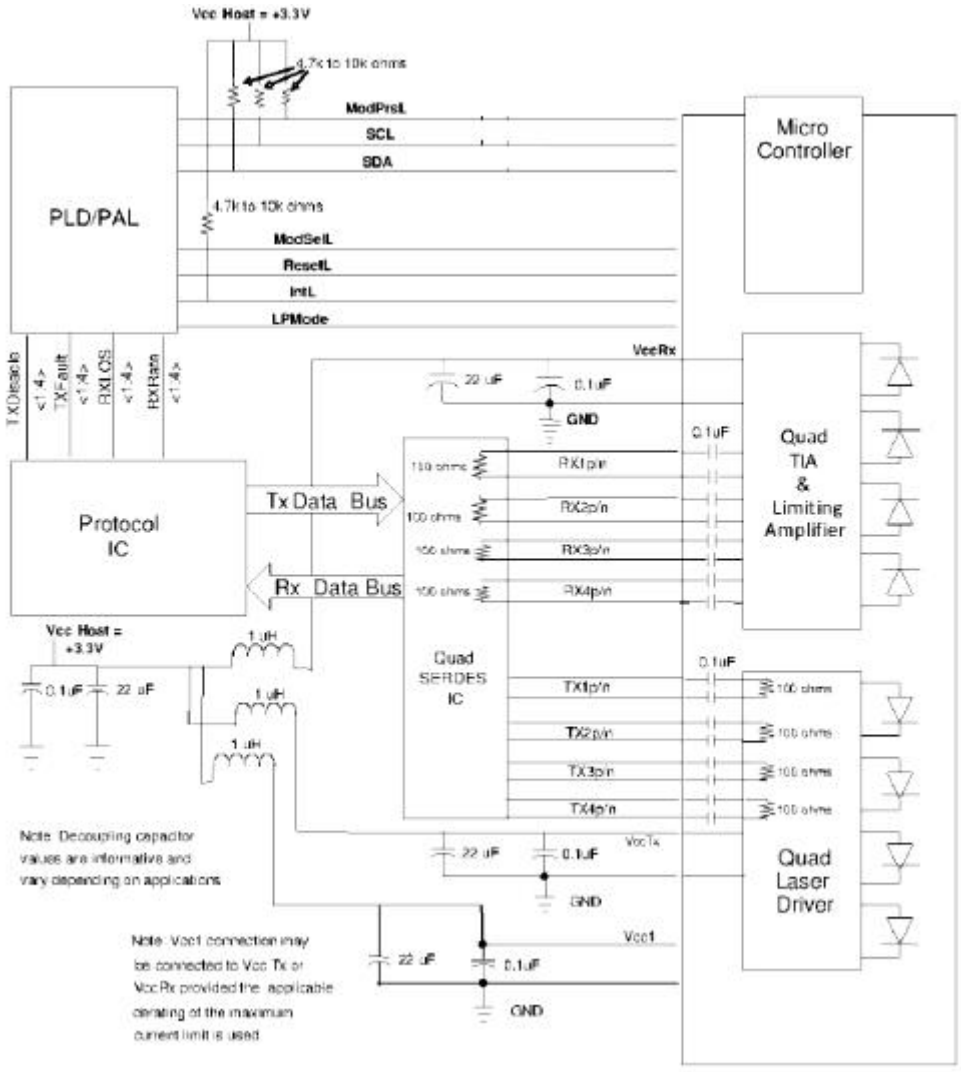
Pin	Symbol	Name/Description	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	

14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	
16	GND	GND	
17	Rx1p	Receiver Non-Inverted Data Output, CML-O	
18	Rx1n	Receiver Inverted Data Output, CML-O	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output, CML-O	
22	Rx2p	Receiver Non-Inverted Data Output, CML-O	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output, CML-O	
25	Rx4p	Receiver Non-Inverted Data Output, CML-O	
26	GND	Ground	
27	ModPrsL	Module Present, connect to GND	
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read.	
29	VccTx	+3.3 V Power Supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I	
34	Tx3n	Transmitter Inverted Data Output, CML-I	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I	
37	Tx1n	Transmitter Inverted Data Output, CML-I	
38	GND	Ground	



Pin-out of Connector Block on Host Board

Recommend Circuit Schematic



Absolute

Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+3.6	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity	RH	15		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc	-	-	600	mA	Commercial
Case Operating Temperature	Tc	0	-	+70	°C	Commercial
Bit Rate Each Lane	Br	25.78 ± 100pm			Gbps	

OM3 multimode fiber (MMF)	Lmax	-	-	70	m	

Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Input differential impedance	Rin	85	100	115	Ω	1
Differential data input swing	Vin, pp		-	900	mV	
TX Disable-High	-	Vcc – 0.8	-	Vcc	V	
TX Disable-Low	-	Vee	-	Vee+ 0.8	V	
TX Fault-High	-	Vcc-0.8	-	Vcc	V	
TX Fault-Low	-	Vee	-	Vee+0.8	V	
Receiver						
Output differential impedance	Rin	85	100	115	Ω	1
Single ended data output swing	Vout, pp	100	600	1200	mV	2
LOS-High	-	Vcc – 0.8		Vcc	V	
LOS-Low	-	Vee		Vee+0.8	V	

Notes:

1. AC coupled.
2. Into 100 ohm differential termination.

Optical Characteristics (TOP=25°C, Vcc=3.3 Volts)

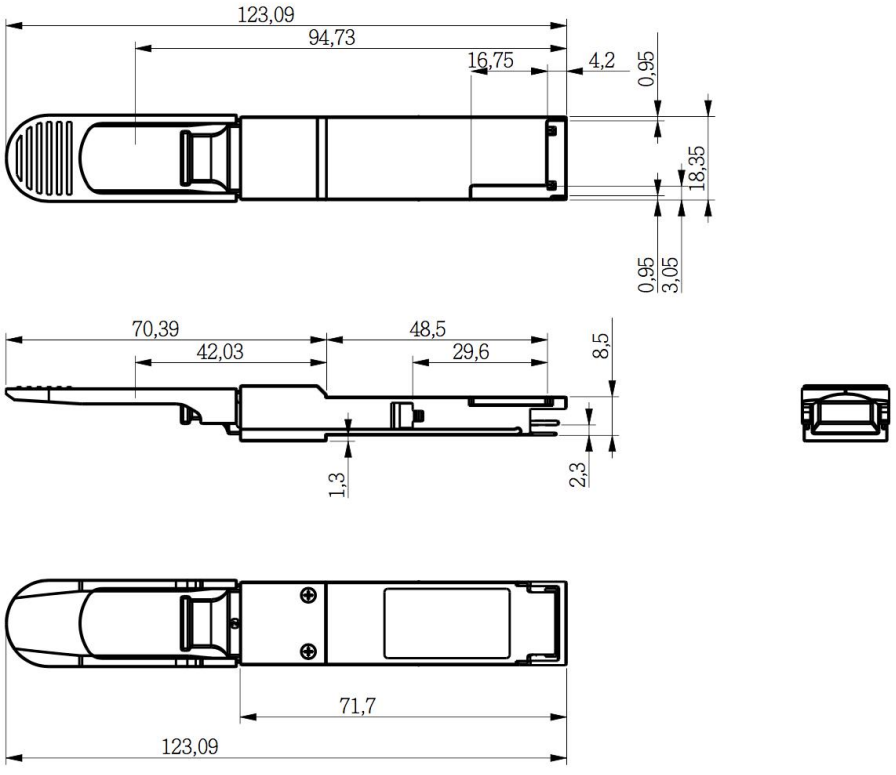
Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Center wavelength		840		860	nm	
RMS spectral width	RMS			0.6	nm	
Average Launch Power, each Lane		-8.4		2.4	dBm	
Optical Modulation Amplitude, each Lane	OMA	-6.4		3	dBm	
Extinction Ratio	ER	2			dB	
Average launch power of OFF	T_{off}			-30	dBm	

transmitter,each lane						
Receiver						
Optical Wavelength		840		860	nm	
Average power at receiver input,each lane	R_{in}	-10.3	-	2.4	dBm	1
Damage threshold		3.4	-	-	dBm	
Optical Modulation Amplitude(OMA),each lane				3	dBm	
Stressed receiver sensitivity in OMA,each lane				-5.2	dBm	
LOS De-Assert	LOSD	-	-	-13	dBm	
LOS Assert	LOSA	-30	-	-	dBm	
LOS Hysteresis	-	0.5	-	-	dB	

Notes:

1. Measured with PRBS 2^{31}-1 at 10-12 BER.

Mechanical Specifications



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EEPROM Information

EEPROM memory map specific data field description is as below:

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Module Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-106 Free Side Device and Channel Mask
107 Reserved
108-112 Free Side Device Properties
113-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h (Cable Assemblies)
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Threshold
192-223 Extended ID			224-225 Reserved
224-255 Vendor Specific ID			226-227 Vendor Specific
			238-241 Channel Controls
			242-253 Channel Monitor Masks
	254-255 Application Code Entry TL		254-255 Reserved

234	7-4	TX1 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
	3-0	TX2 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
235	7-4	TX3 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
	3-0	TX4 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
236	7-4	RX1 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
	3-0	RX2 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
237	7-4	RX3 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 40)	0	0	0	0
	3-0	RX4 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
238	7-4	RX1 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0
	3-0	RX2 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 38)	0	0	0	0
239	7-4	RX3 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0
	3-0	RX4 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0

Code	Page 03H Bytes 234 ~ 235	
	Transmitter Input Equalization	
	Nominal	Units
1100	10.7	dB
1011	10.3	dB
1010	9.8	dB
1001	8.8	dB
1000	8.2	dB
0111	7.2	dB
0110	6.5(Default)	dB
0101	5.3	dB
0100	4.8	dB
0011	3.7	dB
0010	2.7	dB
0001	1.9	dB
0000	1.3	dB
Code	Page 03H Bytes 236~237	
	Receiver Output Emphasis	
	Nominal	Units
1000	7.5	dB

0111	6.5	dB
0110	5.5	dB
0101	4.5	dB
0100	3.5	dB
0011	2.5	dB
0010	1.5	dB
0000	0(Default)	No Emphasis
Code	Page 03H Bytes 238~239	
	Receiver Output Amplitude	
	Nominal	Units
0011	600~1200	mV (p-p)
0010	400~800(Default)	mV (p-p)
0001	300~600	mV (p-p)
0000	100~400	mV (p-p)

Digital Diagnostic Monitoring Interface

Four transceiver parameter values are monitored. The following table defines the Monitory parameter's accuracy.

Parameter	Range	Accuracy	Calibration
Temperature	0 to +70°C	±3°C	Internal
Voltage	2.97 to 3.63V	±3%	Internal
Bias Current	0 to 100mA	±10%	Internal
RX Power	-10.3 to 2.4dBm	±3dB	Internal

Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
V1.0	Chuck.chen	Sun.bin	Ding.zheng	New Released.	Aug. 1, 2017

For More Information

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