



## 100Gb/s QSFP28 Active Optical Cable

### APCO10-PPCXXX

#### ■ Product Features

- ✓ Available in lengths of 1 to 50m on OM3 multimode fiber(MMF)
- ✓ 4 independent full-duplex channels up To 25Gbps data rate per wavelength
- ✓ Hot-pluggable QSFP28 footprint
- ✓ RoHS compliant and Lead Free
- ✓ Power dissipation <2W (0~70°C)
- ✓ Commercial operating temperature optional
- ✓ Compliant with IEEE802.3ca, SFF-8436



#### ■ Applications

- ✓ 100GBASE-SR4
- ✓ 100G Ethernet



■ **Product Selection**

Part Number	Lengths
APCO10-PPC010	1m
APCO10-PPC020	2m
APCO10-PPC030	3m
APCO10-PPC050	5m
APCO10-PPC070	7m
APCO10-PPC100	10m
APCO10-PPC150	15m
APCO10-PPC200	20m
APCO10-PPC250	25m
APCO10-PPC300	30m
APCO10-PPC400	40m
APCO10-PPC500	50m

\*For availability of additional cable lengths, please contact ATOP.

■ **Regulatory Compliance**

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B
- RoHS compliant with RoHS 2 (2011/65/EU)

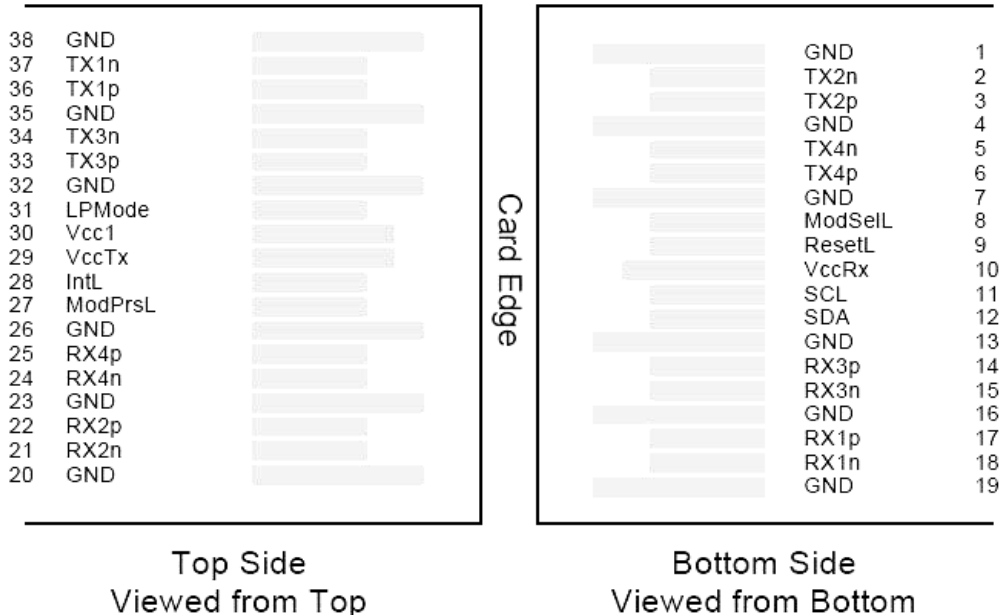
■ **Pin Descriptions**

Pin	Symbol	Name/Description	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	



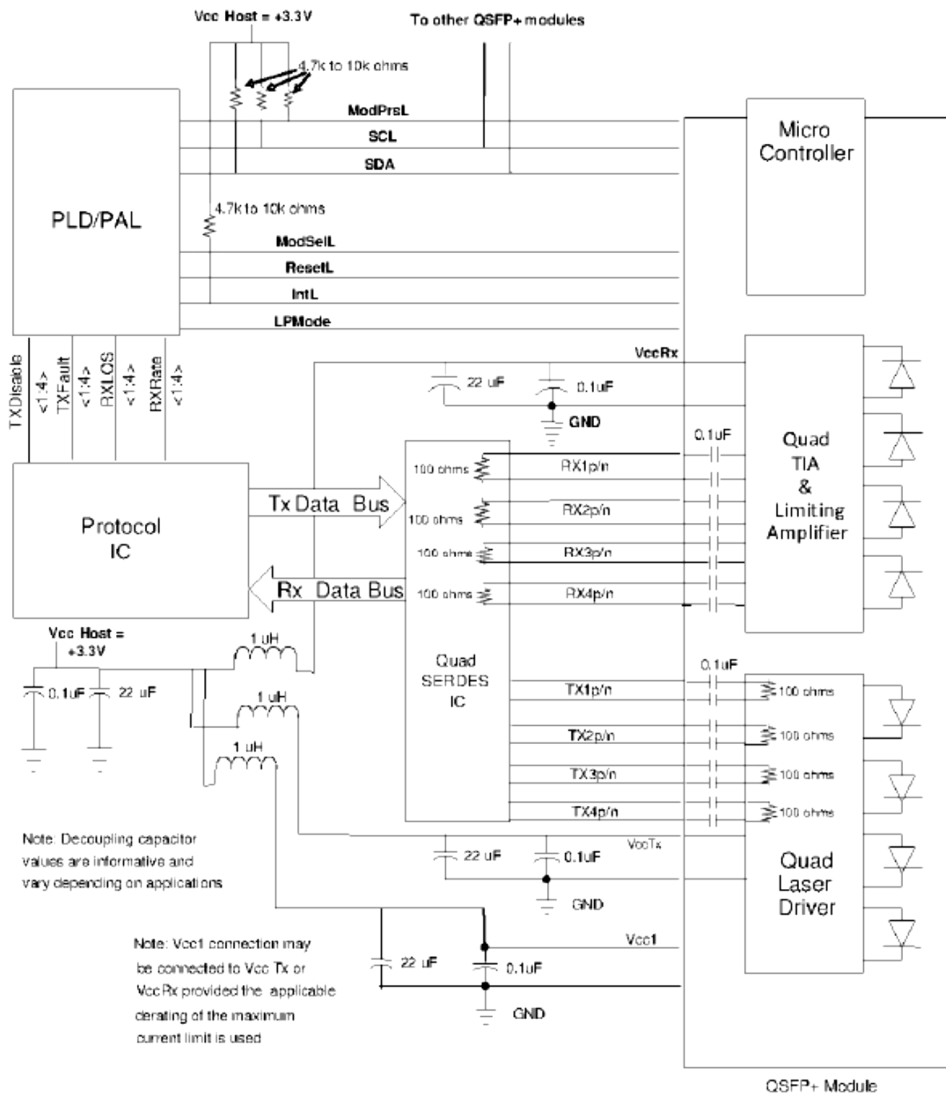
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP28 module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	
14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	
16	GND	GND	
17	Rx1p	Receiver Non-Inverted Data Output, CML-O	
18	Rx1n	Receiver Inverted Data Output, CML-O	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output, CML-O	
22	Rx2p	Receiver Non-Inverted Data Output, CML-O	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output, CML-O	
25	Rx4p	Receiver Non-Inverted Data Output, CML-O	
26	GND	Ground	
27	ModPrsL	Module Present, connect to GND	
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is	

		de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’ and the flag field is read.	
29	VccTx	+3.3 V Power Supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMODE	The LPMODE pin shall be pulled up to Vcc in the QSFP28 module. This function is affected by the LPMODE pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1).	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I	
34	Tx3n	Transmitter Inverted Data Output, CML-I	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I	
37	Tx1n	Transmitter Inverted Data Output, CML-I	
38	GND	Ground	



**Pin-out of Connector Block on Host Board**

■ **Recommend Circuit Schematic**



## Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		+4.0	V	
Storage Temperature	TS	-40		+85	°C	
Operating Humidity	RH	0		85	%	

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	Vcc	3.13	3.30	3.47	V	
Power Supply Current	Icc	-	-	600	mA	Commercial
Case Operating Temperature	Tc	0	-	+70	°C	Commercial
Bit Rate Each Lane	Br	25.78125 ± 100pm			Gbps	



OM3 MMF	Lmax	-	-	50	m	
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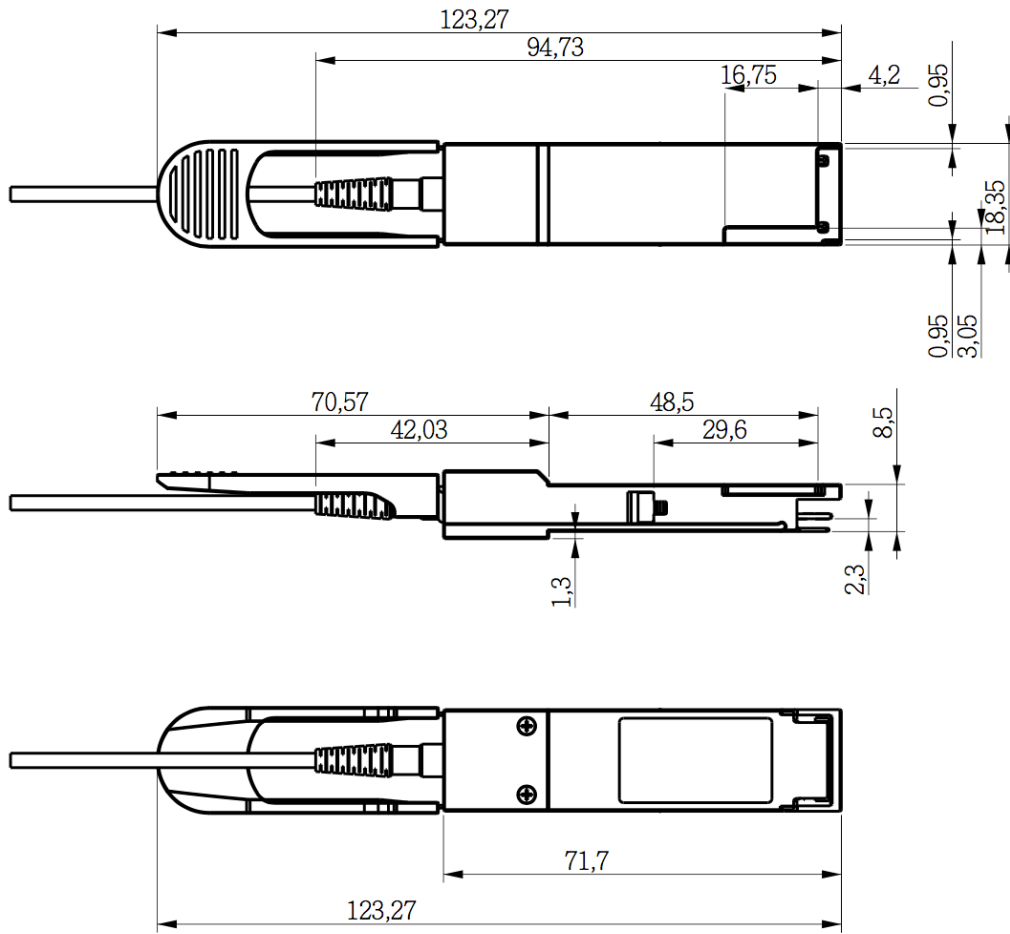
■ **Electrical Characteristics (TOP=25°C, Vcc=3.3Volts)**

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
<b>Transmitter</b>						
Input differential impedance	Rin	80	100	120	Ω	1
Differential data input swing	Vin, pp		-	900	mV	
TX Disable-High	-	Vcc – 0.8	-	Vcc	V	
TX Disable-Low	-	Vee	-	Vee+ 0.8	V	
TX Fault-High	-	Vcc-0.8	-	Vcc	V	
TX Fault-Low	-	Vee	-	Vee+0.8	V	
<b>Receiver</b>						
Single ended data output swing	Vout, pp	100	600	1200	mV	2
LOS-High	-	Vcc – 0.8		Vcc	V	
LOS-Low	-	Vee		Vee+0.8	V	
Pre-FEC Bit Error Ration	BER			10 <sup>-6</sup>		3
Post-FEC Bit Error Ration	BER			10 <sup>-12</sup>		3,4

**Notes:**

1. AC coupled.
2. Into 100 ohm differential termination.
3. Tested with a 231-1 PRBS.
4. Requires FEC on the host to support maximum distance, per 100GBASE-SR4.

■ **Mechanical Specifications**



**APCP10-PPCXXX**

■ **EEPROM Information**

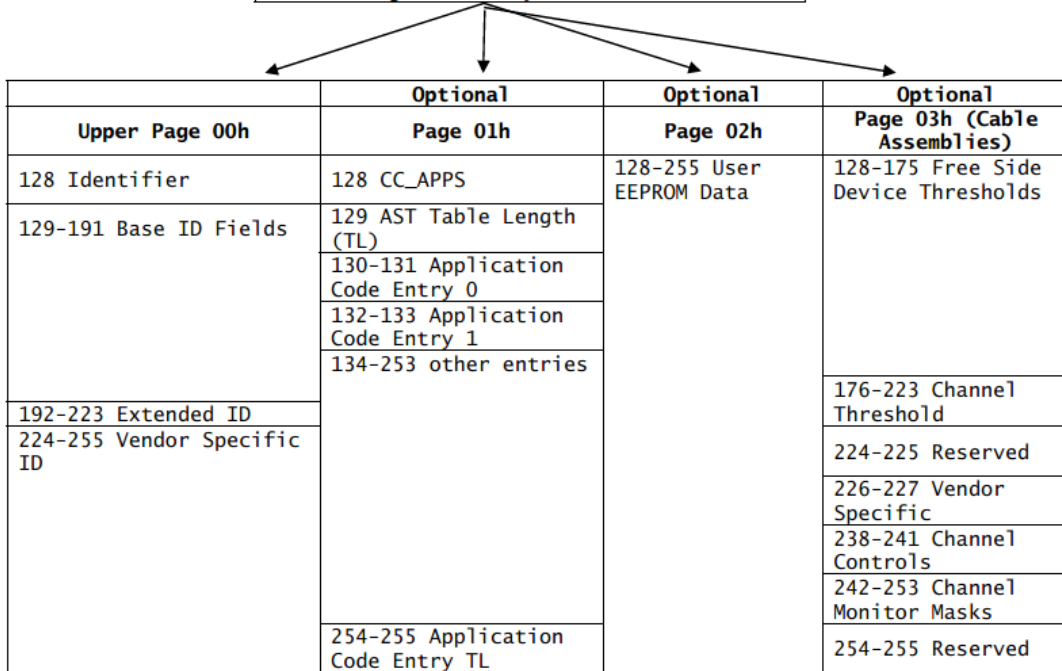
EEPROM memory map specific data field description is as below:

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**APCO10-PPCXXX**

<b>2-Wire Serial Address 1010000x</b>	
<b>Lower Page 00h</b>	
0	Identifier
1- 2	Status
3- 21	Interrupt Flags
22- 33	Module Monitors
34- 81	Channel Monitors
82- 85	Reserved
86- 98	Control
99	Reserved
100-106	Free Side Device and Channel Mask
107	Reserved
108-112	Free Side Device Properties
113-118	Reserved
119-122	Password Change Entry Area (Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte







234	7-4	TX1 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
	3-0	TX2 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
235	7-4	TX3 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
	3-0	TX4 input equalization control	Input equalization level control (see Page 03 Byte 224 and Table 6-33)	0	0	0	0
236	7-4	RX1 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
	3-0	RX2 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
237	7-4	RX3 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 40)	0	0	0	0
	3-0	RX4 output emphasis control	Output emphasis level control (see Page 03 Byte 224 and Table 6-34)	0	0	0	0
238	7-4	RX1 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0
	3-0	RX2 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 38)	0	0	0	0
239	7-4	RX3 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0
	3-0	RX4 output amplitude control	Output amplitude levels with no equalization enabled. (See Table 6-32)	0	0	0	0

Code	Page 03H Bytes 234 ~ 235	
	Transmitter Input Equalization	
	Nominal	Units
1100	10.7	dB
1011	10.3	dB
1010	9.8	dB
1001	8.8	dB
1000	8.2	dB
0111	7.2	dB
0110	6.5(Default)	dB
0101	5.3	dB
0100	4.8	dB
0011	3.7	dB
0010	2.7	dB
0001	1.9	dB
0000	1.3	dB
Code	Page 03H Bytes 236~237	
	Receiver Output Emphasis	
	Nominal	Units
1000	7.5	dB



0111	6.5	dB
0110	5.5	dB
0101	4.5	dB
0100	3.5	dB
0011	2.5	dB
0010	1.5	dB
0000	0(Default)	No Emphasis
Code	Page 03H Bytes 238~239	
	Receiver Output Amplitude	
	Nominal	Units
0011	600~1200	mV (p-p)
0010	400~800(Default)	mV (p-p)
0001	300~600	mV (p-p)
0000	100~400	mV (p-p)

■ Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
V1.0	Chuck.chen	Sun.bin	Ding.zheng	New Released.	Aug. 1, 2017

■ For More Information

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